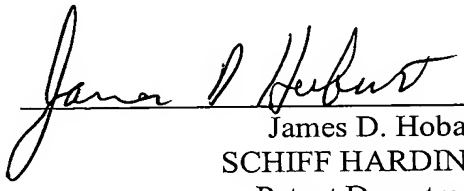
REMARKS

Claims 21-40 are presented for examination.

By this amendment, the Abstract has been amended to remove claim language. A marked-up version of the Abstract is provided in the attached appendix. The specification has been amended to insert headings and to correct grammatical and typographical errors. These changes are included in the attached Substitute Specification and a marked-up version is provided in the appendix. It is respectfully submitted that the Substitute Specification does not include any new matter and is supported by the PCT Application as originally filed.

Claims 1-20, which are on pages 9-12 of the translation, have been redrafted and presented as new claims 21-40 to place them in form for examination in the United States Patent Office and to remove multiple dependency. It is submitted that claims 21-40 are patentable over the references cited in the International Search Report and the additional references provided in the Information Disclosure Statement.

Respectfully submitted,



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ABSTRACT OF THE DISCLOSURE

For hermetic encapsulation of a component, which includes a chip with component structures applied on a substrate in a flip-chip construction, a material is applied onto the lower edge of the chip and regions of the substrate abutting the chip, and then a first continuous metal layer is applied on the back side of the chip and on the material, as well as on edge regions of the substrate abutting the material. For hermetic encapsulation, a second sealing metal layer is subsequently applied by a solvent-free process at least on those regions of the first metal layer that cover the material.

Appendix

TITLE

METHOD FOR HERMETIC ENCAPSULATION OF A COMPONENT

Background of the Invention

A method for hermetic encapsulation of a component is, for example, known from WO 99/43084. There components, in particular surface wave components, are applied in a flip-chip technique to a substrate provided with solderable connection areas. The component, which is fashioned on the chip, is thereby soldered to the substrate over bumps (solder balls) at a slight distance from the substrate, such that the component structures located on the chip face the substrate. For hermetic encapsulation of the components located on the substrate, said components are ultimately covered from the back with a metal foil or a metal-coated plastic film (first metal layer) on the substrate and glued or laminated. The foil thereby seals tight with the substrate between the components, such that an encapsulation is created for the component structures.

After the application of the electrical component on the substrate, the lower edge of the chip and regions of the substrate abutting the chip are frequently covered with a material (under filler), for example organosilic compound or epoxy resin filled with quartz, on which the first metal layer mentioned above is subsequently applied. In another embodiment, for example, a plastic film is applied on the back side of the component chip and regions of the substrate abutting the component, and the film is subsequently sealed with the substrate. The first metal layer is subsequently applied on this film.

In order to tightly encapsulate the component, a second metal layer is normally deposited galvanically or, respectively, without current on this first metal layer. During this galvanic process, small quantities of water can penetrate into the electrical component. This water can lead to long-term corrosion of the electrical component. Until now, after the galvanic reinforcement of the first metal layer, this moisture has only been homogenously distributed in the component via a tempering step at ~~(typically)~~ a typical temperature of 125°C, without completely removing ~~it~~ the moisture from said component.

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Summary of The Invention

It is therefore the object of the invention to specify a method for hermetic encapsulation of an electrical component which is simple to implement and prevents the disadvantages cited above.

~~This object is inventively achieved via a method according to claim 1. Advantageous embodiments of the method are the subject matter of sub-claims.~~

The invention proposes to first apply a component fashioned on a chip onto a substrate in a conventional flip-chip construction (method step A) and to subsequently cover at least the lower edge of the chip and regions of the substrate abutting the chip with a material in a conventional manner in method step B). In method step C), a first continuous metal layer is subsequently applied on the back side of the chip, on the material and on edge regions of the substrate abutting the material. A second hermetically sealing metal layer that ~~covvers [sic]~~ covers the material is subsequently, inventively applied, at least on the regions of the first metal layer, whereby this second metal layer is applied by means of a solvent-free and in particular water-free process (method step D). An electroplating using water-free organic solvent is alternatively also possible.

In contrast to the prior art, the second metal layer is ~~therewith~~ not applied by means of a galvanic process in which water as solvent penetrates into the component and can ~~therewith~~ cause a corrosion of the component. Furthermore, the second metal layer is not applied on all regions on which the first continuous metal layer is present, but rather only on those regions of the first metal layer that cover the insulating material. This has the advantage that, in the inventive method, the consumption of the metal can be significantly reduced for the second metal layer.

A whole series of processes are considered for a solvent-free process in the method step B) to apply the second hermetically sealing metal layer. Thus, for example, it

is possible to melt a metal foil onto the first metal layer. Before the application, this metal foil is ~~thereby~~ advantageously adapted (stamped) to the contours of the first metal layer, such that it attaches to the first metal layer with a positive fit. This has the advantage that, upon melting of this metal foil on the first metal layer, the second metal layer is generated with homogenous layer ~~thikkness [sic]~~ thickness, such that it particularly tightly seals the component.

Furthermore, it is possible that metal particles are applied in the method step D). This can, for example, be implemented with the aid of a spray method in which the fluid metal beads are sprayed. Furthermore, in a further embodiment of the inventive method a metal paste can be applied and then baked. The second metal layer can also be applied by means of chemical vapor deposition (CVD) or physical vapor deposition (PVD). Furthermore, the second metal layer can also be sputtered or deposited galvanically or without current with a water-free electrolyte.

The second metal layer can be applied continuously onto the first metal layer. In this case, the second metal layer thus covers not only those regions of the first metal layer that cover the material, but rather also further regions of the first metal layer that, for example, cover the back side of the chip.

In a further advantageous variant of the inventive method, before the application of the second metal layer a surface layer of the first metal layer can be removed to improve the bonding. Due to oxidation processes, a metal oxide layer to which the second metal layer bonds only in a limited manner frequently forms on the first layer. For this reason, this oxide layer is advantageously removed, for example via a reducing hydrogen plasma, before the application of the second metal layer.

In another embodiment of the inventive method, in the method step B) the material is, for example, applied in the form of a plastic film, such that the plastic film covers the back side of the chip and simultaneously the edges of the film overlap the chip. The film is subsequently sealed with the substrate in the entire edge

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region around the chip. The first metal layer is then applied onto this plastic film in the further method step C). This variant of the inventive method has the advantage that the method steps B) (application of the plastic film) and the method step C) (application of the first continuous metal layer) can be particularly well optimized independent of one another. In cooperation with the last method step D), a particularly secure hermetic encapsulation of the electrical component is thus possible via the application of the second metal layer. In this variant of the inventive method, the second hermetically sealing metal layer is advantageously applied over the entire first continuous metal layer. It is thereby particularly advantageously ensured that, in components encapsulated according to this variant, no moisture can penetrate through both metal layers into the plastic film, and thus also into the component.

In a further variant of the inventive method, the metals for the first and second metal layer and the process conditions for the application of the second metal layer in the method step D) are selected such that, during the application of the second metal layer, a metal alloy with a melting point of more than 260°C is formed at the boundary area between the two metal layers. This has the advantage that the metal alloy does not melt, and therefore is also not permeable or loses rigidity, upon soldering of the inventively encapsulated component, which normally ensues at temperatures below 260°C. Such encapsulated component can thus be soldered without large problems as SMD components by means of standard soldering methods.

As a first metal layer, a titanium-copper layer is advantageously applied in which a thicker copper layer is applied as a bonding agent to a very thin titanium layer. As a second metal layer, tin or ~~eutectics (such as~~ eutectic tin alloys, for example, tin-silver, tin-copper or tin-silver copper alloys or a mix of the cited ~~metals~~ metals are advantageously applied. This has the advantage that the cited metals or, respectively, metal alloys are very inexpensive for the first and second metal layer, but at the same time a non-eutectic tin-copper alloy with a melting point of greater than 260°C is formed at the

boundary area between the first metal layer and the second metal layer upon application of the second metal layer. By means of this variant of the inventive method, it is thus particularly advantageously possible to generate, by means of inexpensive output materials for both of the metal layers, an alloy with a particularly high melting point that can not be melted during standard soldering methods at standard temperature. The materials cited above for the second metal layer thereby exhibit melting points between approximately 217°C and 232°C before the alloy formation.

In another variant of the inventive method, it is also possible to apply a metal layer from the start in method step D) that exhibits a melting point greater than 260°C. For example, tin-gold alloys with melting points of approximately 280°C are considered for this alternative.

The inventive method can be used for a hermetic encapsulation of the most varied components that can be mounted in flip-chip configuration, for example surface wave filters or other (~~and in~~ particular surface-sensitive) components.

In the following, the inventive method should be explained in further detail using Figures.

Brief Description of the Drawings

Figure 1 shows the first method step or method step A) of the inventive method.

Figures 2A and 2B show two ~~embodiment variants~~ embodiments or variations of the second method step or method step B).

Figures 3A and 3B show both components shown in 2A and 2B after the third method or method step C) of the inventive method.

~~In~~ Figures 4A and 4B show ~~, the~~ electrical component ~~is visible~~ after the fourth method step or method step ~~C),~~ D), which is the application of the second metal layer.

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Figure 5 shows the formation of an ~~An~~ alloy with high melting point ~~formed~~ between the first metal layer and second metal layer ~~is visible in Figure 5.~~ ; and

Figures 6 through 8 show the division of the substrate between two components that have been applied, contacted and encapsulated on the substrate according to the method steps A) through D).

Description of the Preferred Embodiments

Figure 1 shows an electrical component after the method step A). It is visible that a chip 1 is attached and contacted on a substrate 25 such that the component structures 5 located on the surface face ~~point to~~ the substrate 25. Solder balls 10 (bumps) thereby affix the component at a slight distance from the substrate and simultaneously electrically-conductively connect the connection areas 20 located on the substrate 25 with the component. A feedthrough 15 thereby provides for electrical contact between the connection areas 20 and the bumps 10.

Figure 2A shows a variant of the method steps B) of the inventive method. A plastic film 30 is continuously applied over the back side of the chip 1 and the regions of the substrate 25 abutting the chip, and has subsequently been sealed with the substrate in the entire edge region of the chip. An embodiment alternative to Fig. 2A is visible in Figure 2B. The space between lower edge of the chip 1 and the regions of the substrate abutting thereon have been covered with a material 35. This material can, for example, be ~~comprised~~ formed of silicon-organic compounds.

The component shown in Figure 2A is visible in Figure 3A after the method step C). The first metal layer 40, for example a titanium-copper layer, has been applied on the plastic film 30. Figure 3B likewise shows the component shown in Figure 2B after the method step C). In this case, the first metal layer 40 has likewise been applied on the material 35 and the back side of the chip. The first metal layer 40 can, for example, be sputtered.

MARKED-UP VERSION

Figure 4A shows the component from Figure 3A after the application of the second metal layer (method step D). In this case, the second metal layer has been applied on the first such that the first metal layer is completely covered by the second metal layer. Figure 4B likewise shows the component shown in Figure 3B after the method step D). In this embodiment, the second metal layer is applied only on those regions of the first metal layer that cover the material 35, which is sufficient for encapsulation.

Figure 5 shows a layer 50 that has been formed on the boundary area of the first metal layer 40 and the second metal layer 45 upon application of the second metal layer 45. This intermediate layer 50 advantageously exhibits a melting point of greater than 260°C, such that the inventive encapsulation of the component no longer melts upon soldering. If a titanium-copper layer is applied as a first layer, either tin or eutectic tin alloys, for example, tin-silver, tin-silver-copper or tin-copper alloys, can advantageously be used as a second layer. These eutectics exhibit a homogenous composition and have defined melting points of approximately 217°C to 232°C. If the second metal layer is applied on the first metal layer at temperatures greater than approximately 280°C, thus the melting point of tin/gold, a non-eutectic tin-copper alloy that exhibits a melting point greater than 260°C forms via bonding of parts of the copper of the first layer with component parts of the second layer. This non-eutectic alloy comprises larger portions of copper than the copper-containing eutectic alloys cited above.

Figure 6 shows a plurality of components that have been applied, contacted and encapsulated on the substrate according to the method steps A) through D). It is thereby possible with the inventive method to apply and to encapsulate identical or different components on the substrate. The chips can subsequently be isolated at the dividing lines designated with 55. For this, as shown in Figure 6 the second metal layer can be ablated, for example by means of a laser, in the region in which the substrate 25 is sectioned.

Figure 7 shows how the first metal layer 40, which has been uncovered due to the laser method cited above, is removed by means of a selective chemical etching. Thus, for example, it is possible to use an iron chloride solution that selectively etches the first metal layer 40 ~~comprised~~ which is formed of titanium and copper, without attacking the second metal layer 45 ~~comprised~~ which is formed of tin or, respectively, tin alloys. After the removal of the first and second metal layer, the chips can, for example, be isolated via sawing of the substrate, as shown in Fig. 8.

The invention is not limited to the exemplary embodiments shown here. Further variations are possible, both with regard to the materials for the first and second metal layer and with regard to the type of the encapsulated components.

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We claim:

~~-Patent claims~~

1. Method for production of an encapsulated encapsulation for an electrical component with the method steps:

A) a component with metallizations fashioned on a chip (1) is attached to a substrate (25) that comprises electrical connection areas (20), whereby the surface of the chip (1) bearing component structures (5) faces the substrate and bump connections (10) that electrically connect the metallizations with the connection areas affix the chip at a slight distance from the substrate,

B) a material (35) is applied such that it covers at least the lower edge of the chip the regions of the substrate abutting the chip,

C) a first, continuous metal layer (40) is applied on the back side of the chip, on the material (35) and on edge regions of the substrate abutting the material,

D) a second, hermetically sealing metal layer (45) is applied by means of a solvent-free process at least on regions of the first metal layer (40) that cover the material (35).

2. Method according to the preceding claim,

- in that a metal foil is melted onto the first metal layer (40) in method step D).

3. Method according to the preceding claim,

- in that the shape of the metal film is adapted to the contours of the first metal layer (40) before the application, such that it lies on the first metal layer with positive fit.

4. Method according to claim 1,

- in that metal particles are applied and then melted in the method step D).

5. Method according to claim 1,

MARKED-UP VERSION

Abstract of the Disclosure

~~Method for hermetic encapsulation of a component~~

For hermetic encapsulation of a component which includes a chip with component structures applied on a substrate ~~(25)~~ in a flip-chip construction, ~~said component comprising a chip (1) with component structures (5), it is proposed to apply~~ a material ~~(35)~~ is applied onto the lower edge of the chip and regions of the substrate abutting the chip, and ~~to apply thereon~~ then a first continuous metal layer ~~(40)~~ is applied on the back side of the chip and on the material ~~(35)~~, as well as on edge regions of the substrate abutting the material. For hermetic encapsulation, a second sealing metal layer ~~(45)~~ is subsequently applied ~~(by means of~~ by a solvent-free ~~process)~~ process at least on those regions of the first metal layer ~~(40)~~ that cover the material ~~(35)~~.

~~Fig. 4B.~~